

FIG. 1

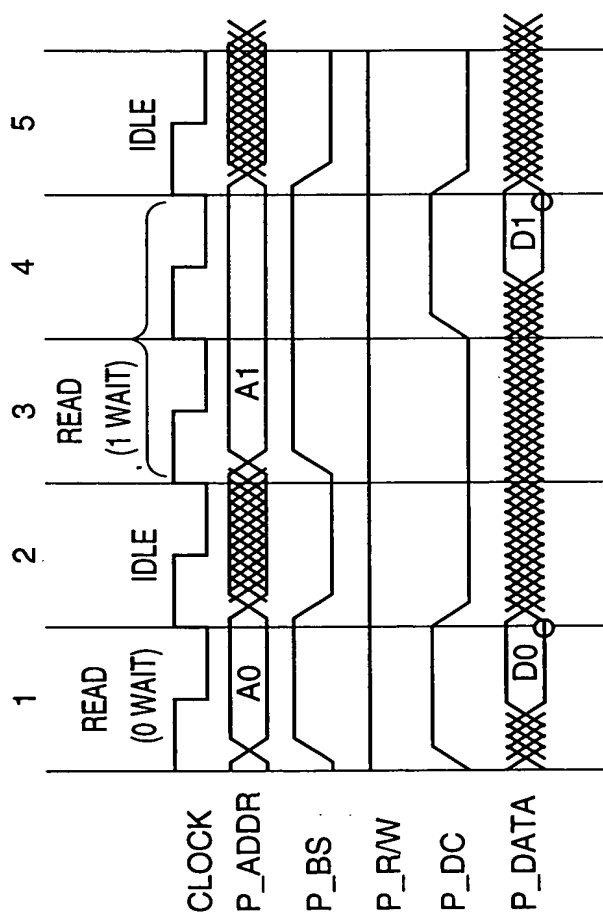


FIG. 2

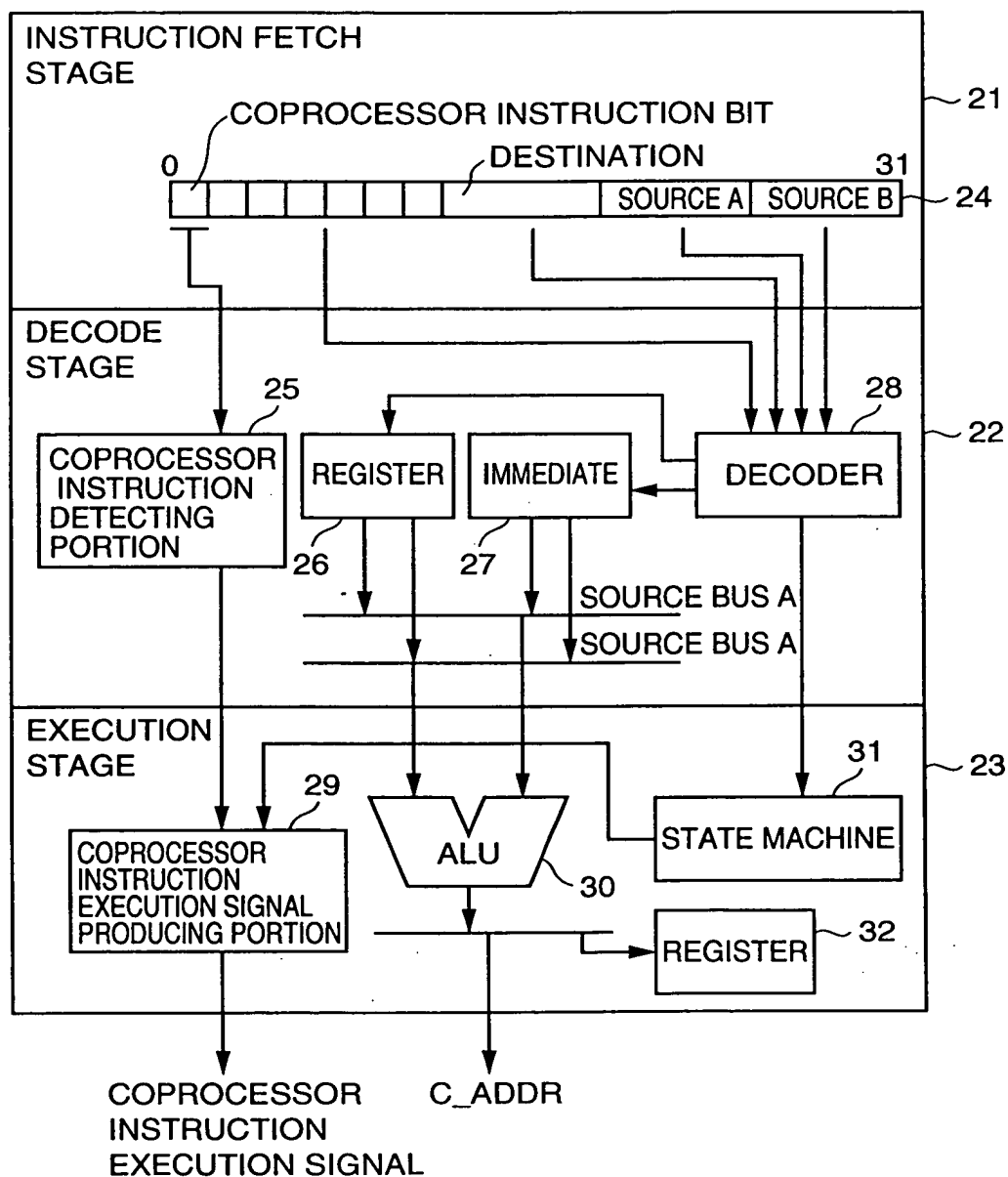
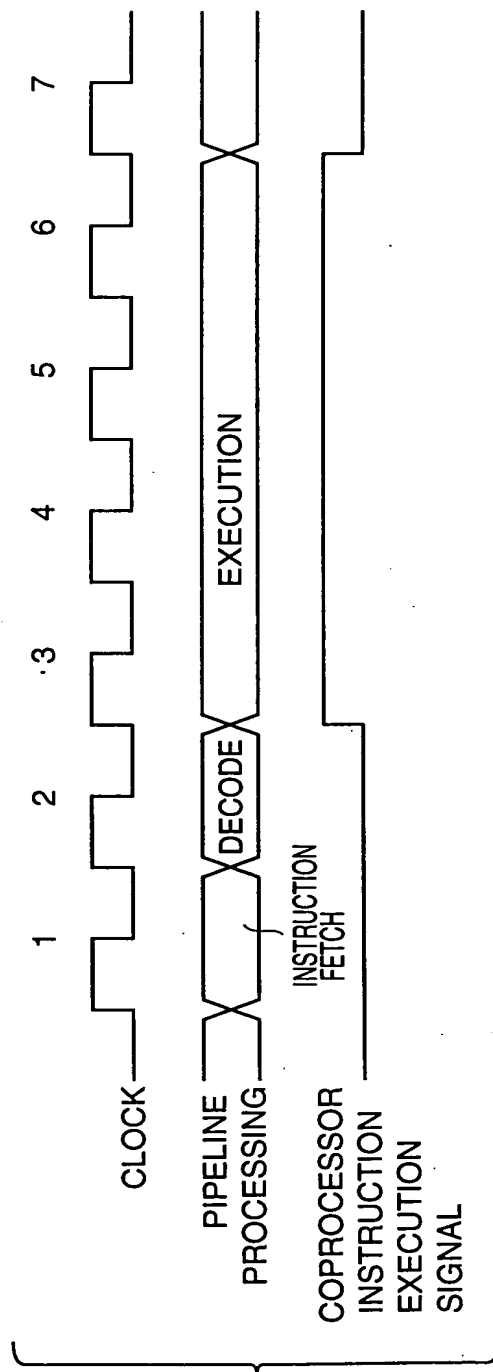


FIG. 3

FIG. 4



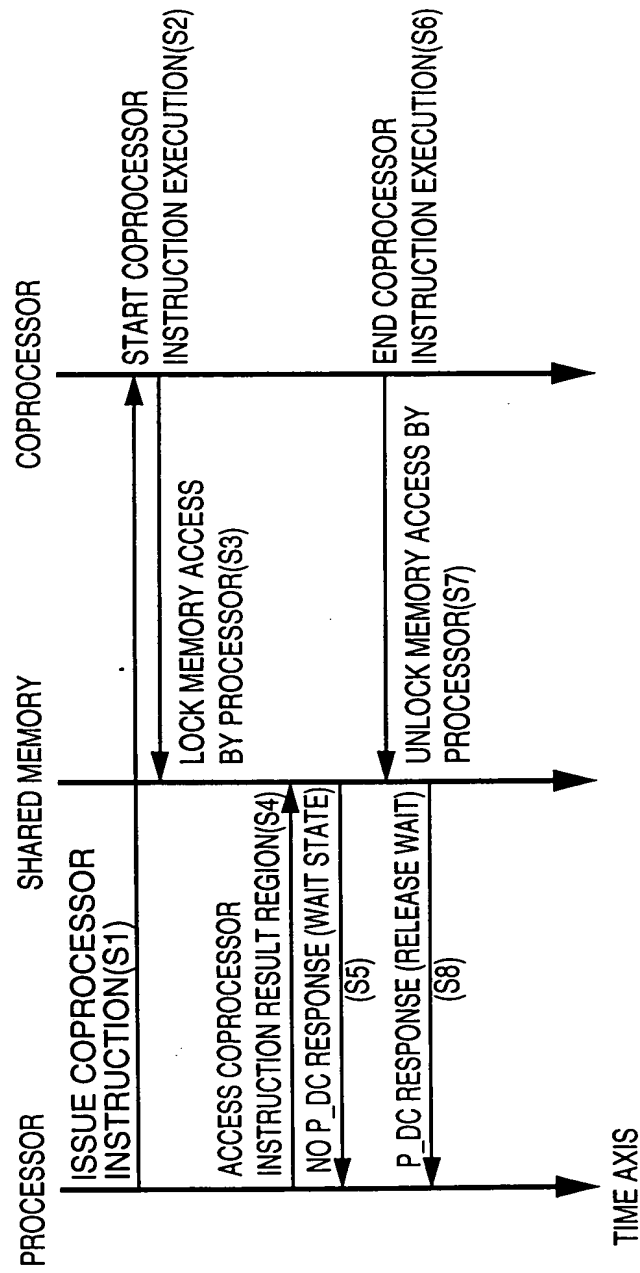


FIG. 5

FIG. 6

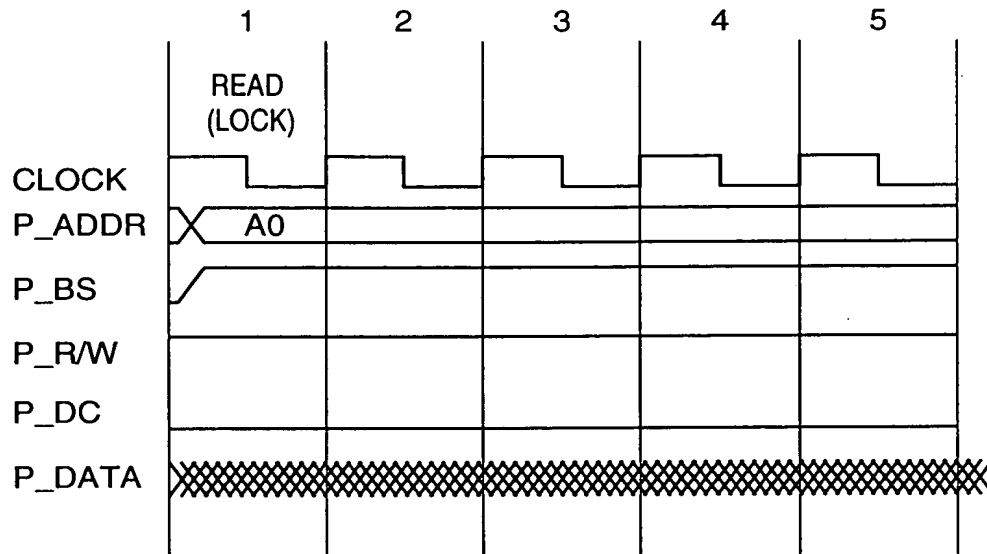
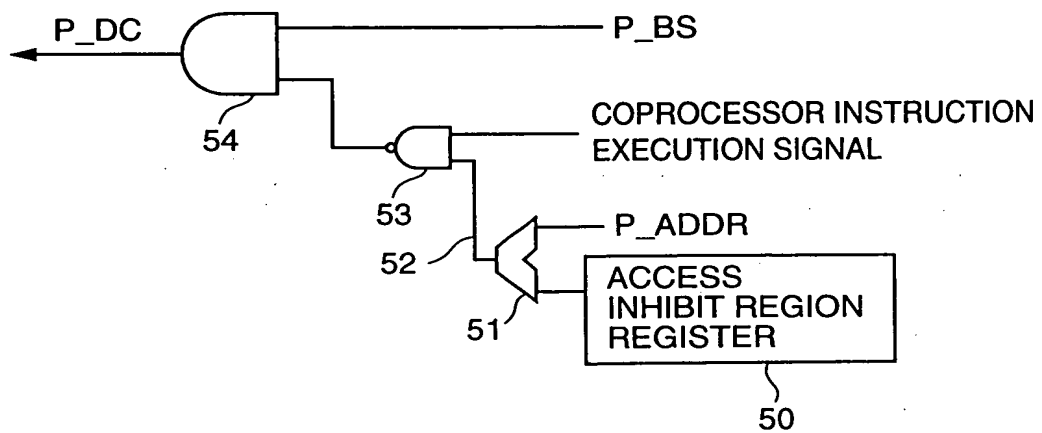


FIG. 7



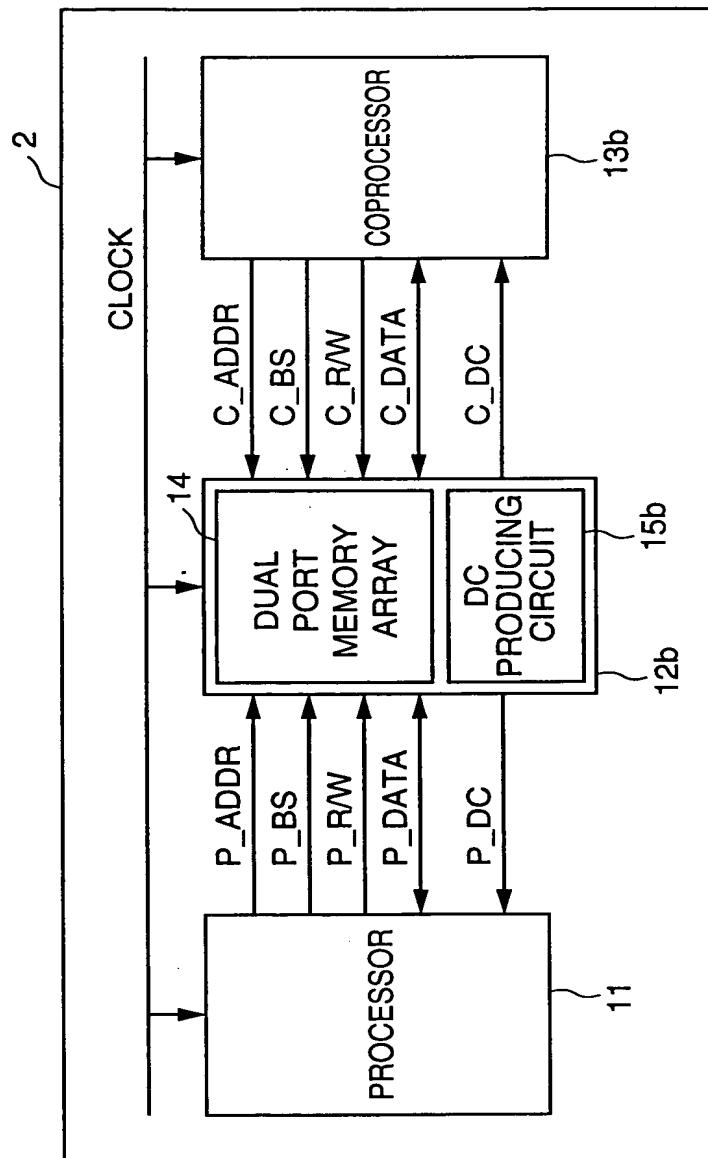


FIG. 8

FIG. 9

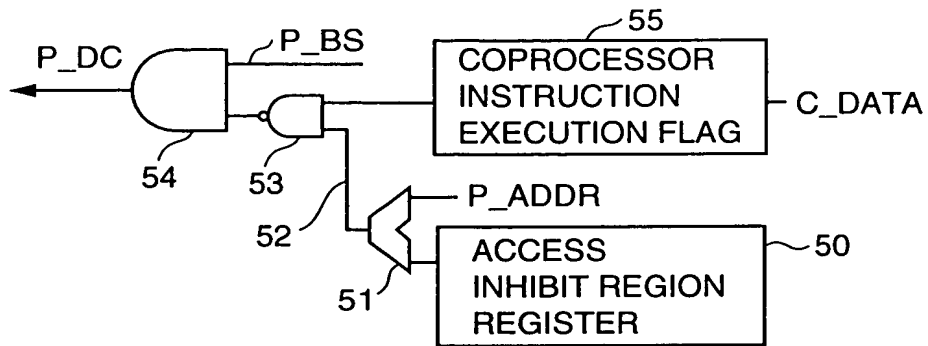
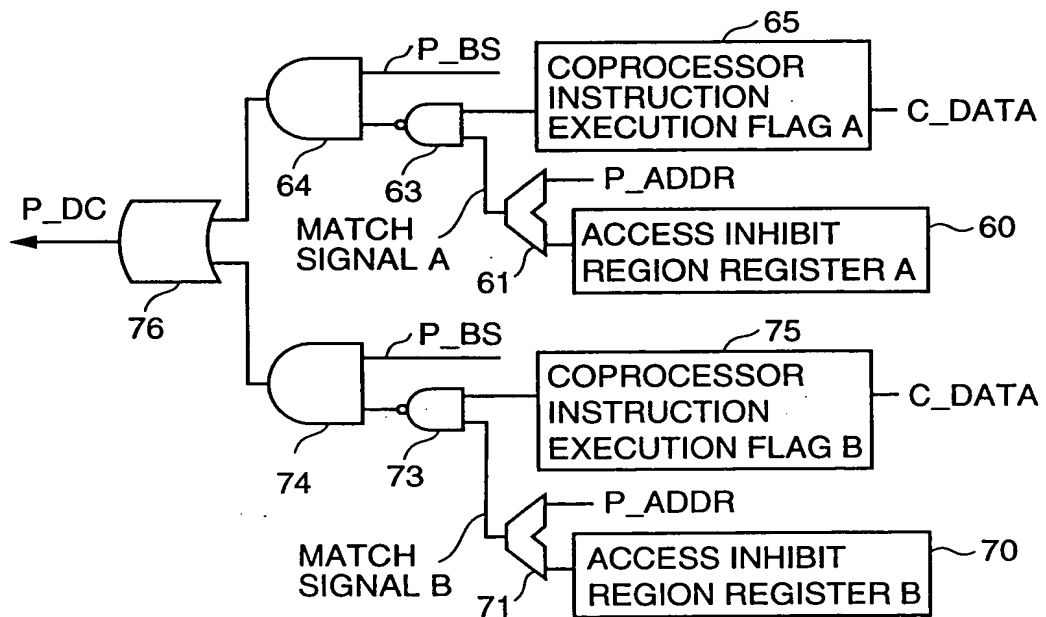


FIG. 10



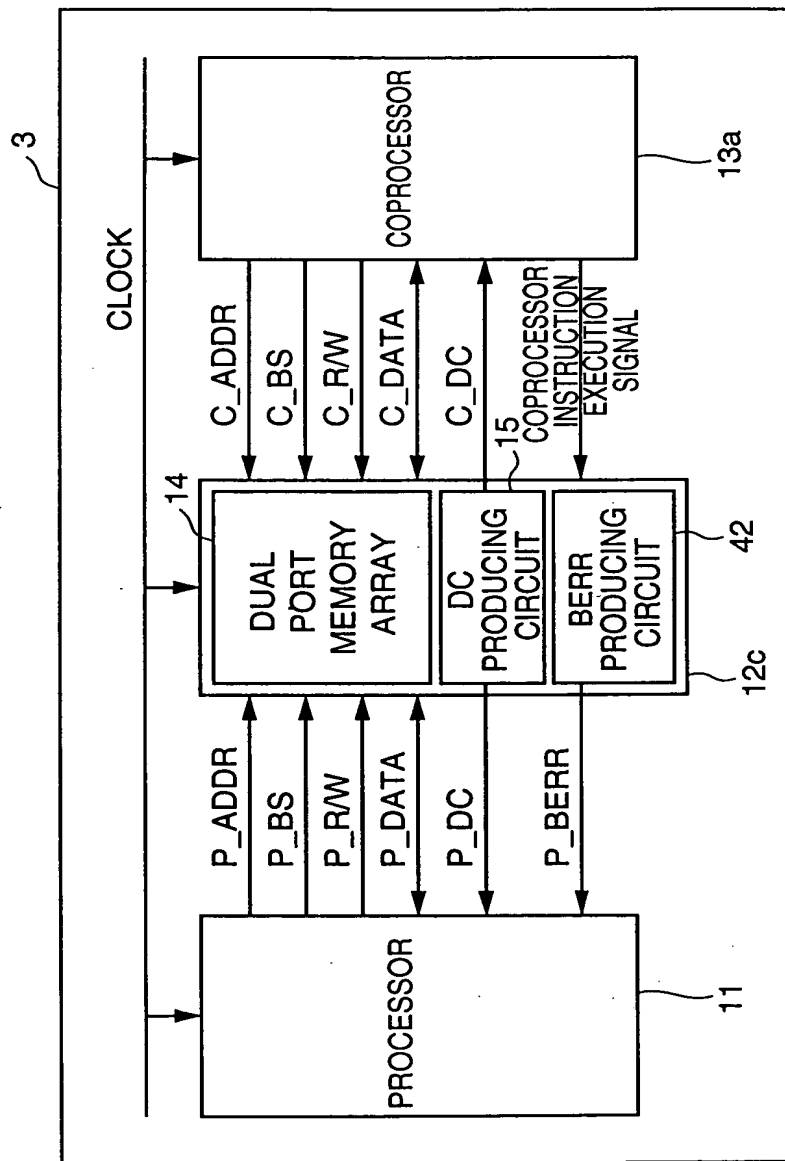


FIG. 11

FIG. 12

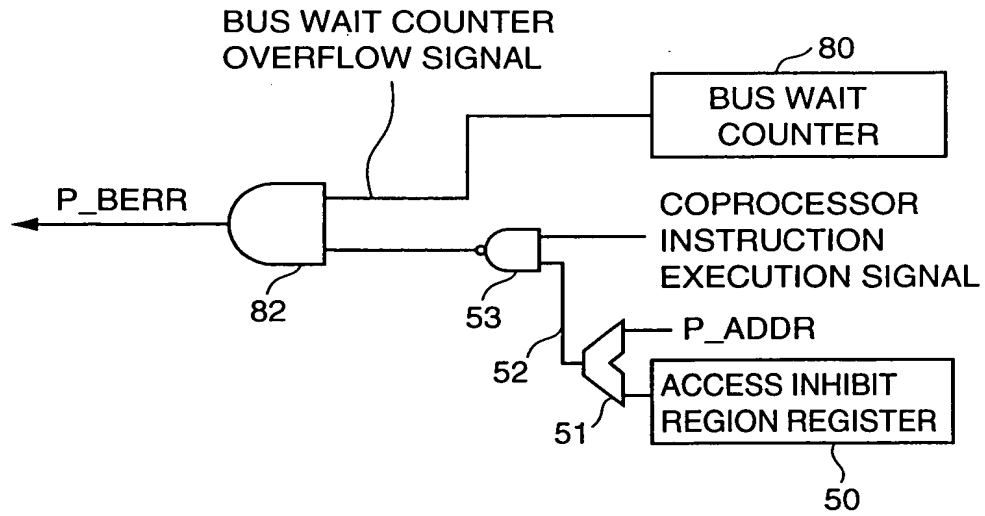
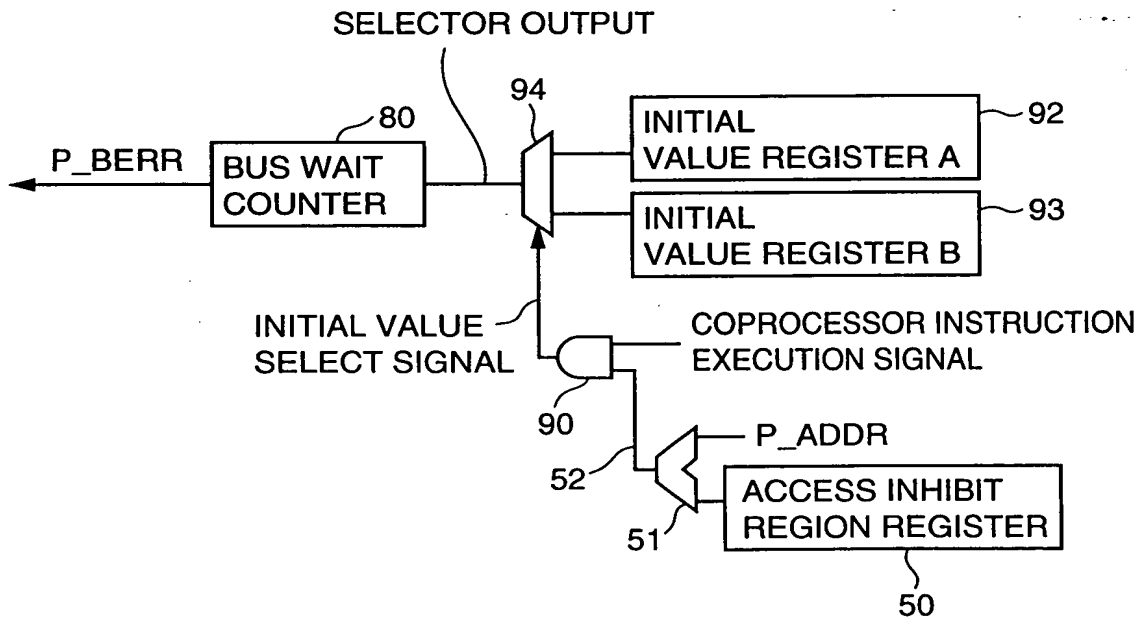


FIG. 13



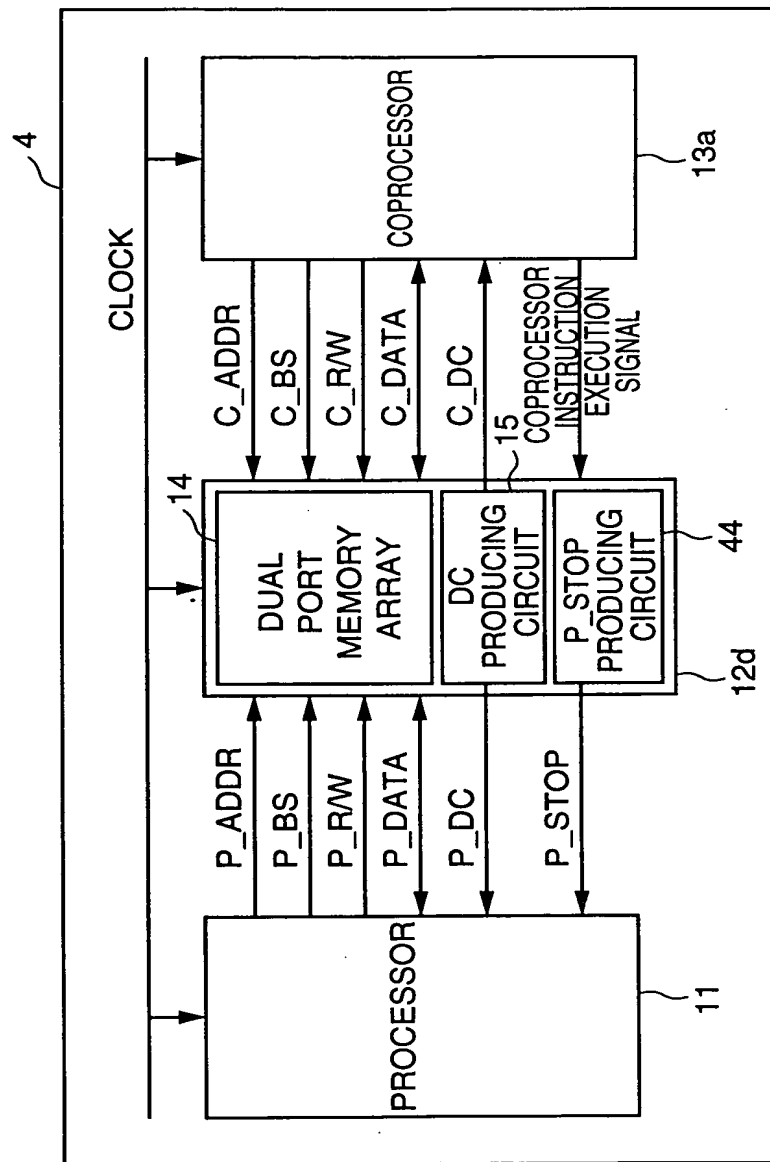


FIG. 14

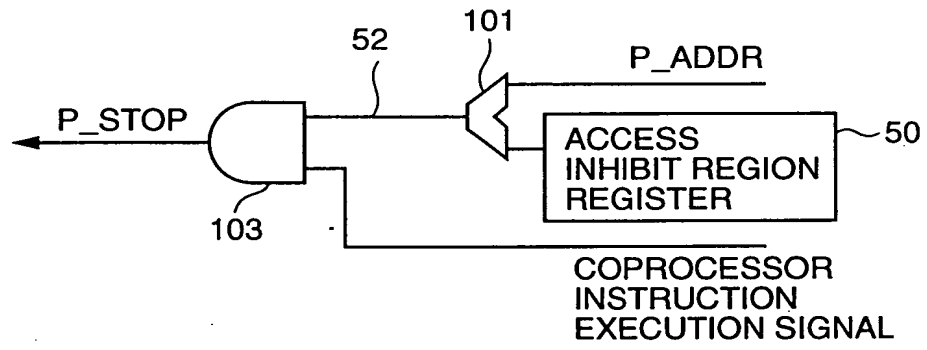


FIG. 15

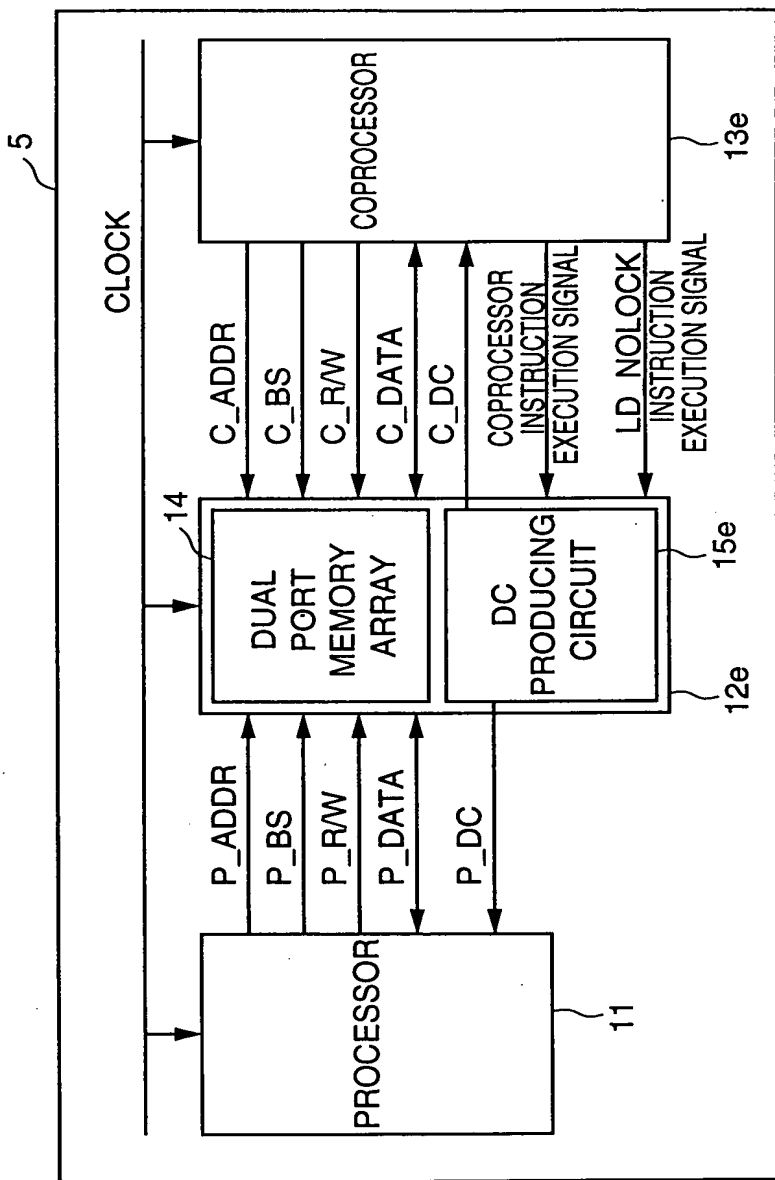


FIG. 16

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graph LR
    P_DC --> 111
    LD_NOLOCK --> 111
    LD_NOLOCK --> 110
    111 --> P_BS
    110 --> 53
    53 --> 51
    52 --> 51
    51 --> 50[ACCESS INHIBIT REGION REGISTER]
  
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Figure 1 is a schematic diagram of an access inhibit region register control circuit. The circuit includes an AND gate 111 with inputs P_DC and LD_NOLOCK, outputting P_BS. LD_NOLOCK is also an input to OR gate 110. The output of 110 is an input to AND gate 53. The output of 53 is an input to OR gate 51. OR gate 51 also receives input 52 and outputs to the ACCESS INHIBIT REGION REGISTER 50.

FIG. 17

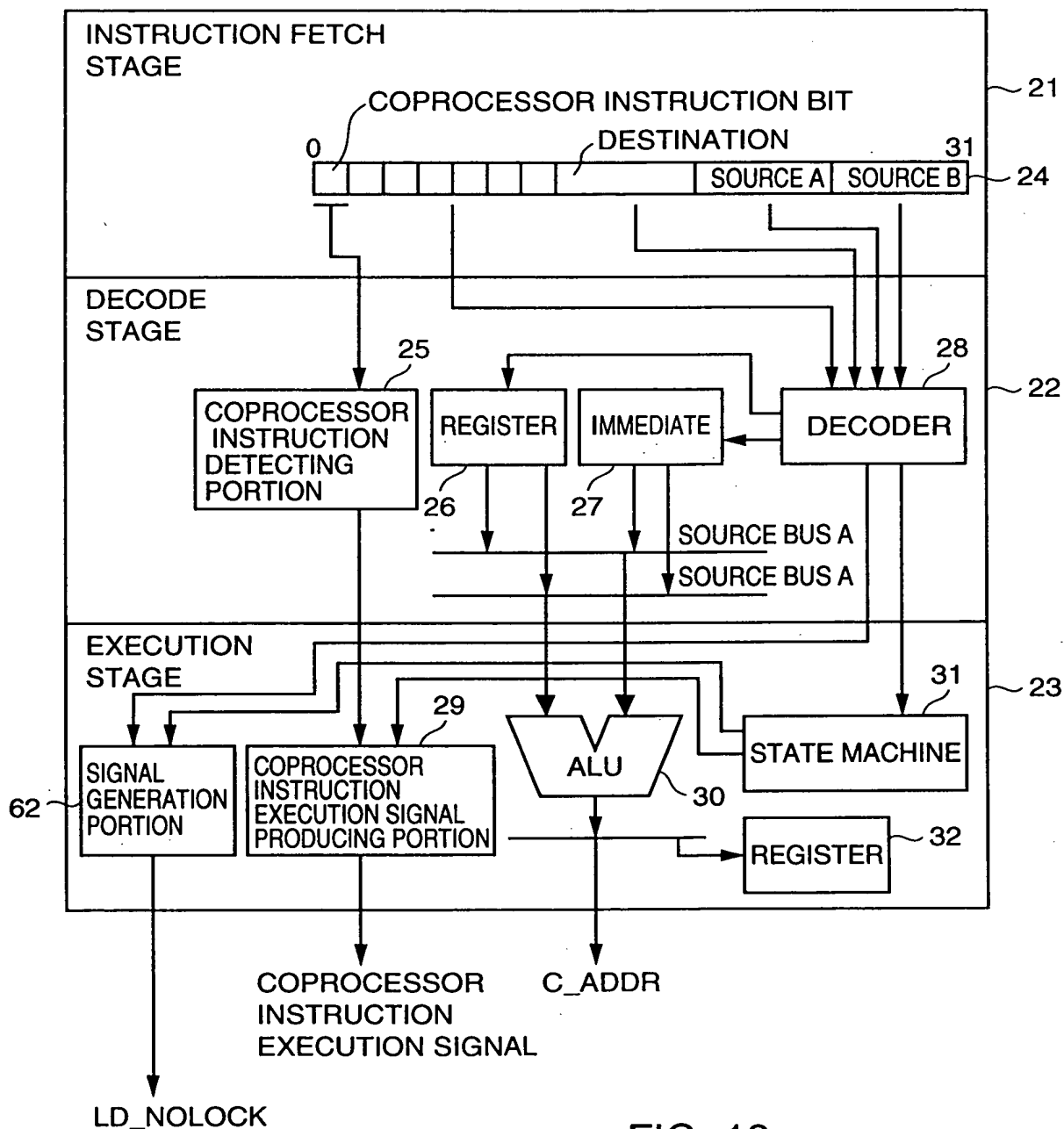


FIG. 18